In the Specification

Please amend the Specification as follows.

In the paragraph beginning at page 6 line 28:

The second category of errors are errors correctable using error handling routines in ~~PAL 101 201, SAL 102, and OS 103~~ PAL 201 and SAL 202, and is shown at 102. This error type is sometimes called "continuable error with firmware correction". Typically, any processes executing on a detecting processor are interrupted and information necessary to resume the these processes is stored in a log. The error handling routines in these layers can be used to correct the error and the processes can resume execution. The resumed processes are unaware of the error or the interruption. An example of this type of error is a parity error in the processor instruction cache. In this case, firmware will invalidate the entire instruction cache, access another copy of the instruction, and resume execution of the interrupted process. This type of error can be signaled to a processor by the platform via a double bit ECC error on the system bus.

In the paragraph beginning at page 11 line 12:

The processor 304 and platform hardware 305 can detect errors and attempt to correct them. Errors that affect only one processor are local errors. Errors that ~~effect~~ affect more than one ~~error~~ processor are global errors. If the processor 304 is unable to correct the error, error handling is handed off to PAL 301. On detecting an interrupt, a signal or interrupt is generated to allow other system software to be aware of the error.